FIG. 1(A)

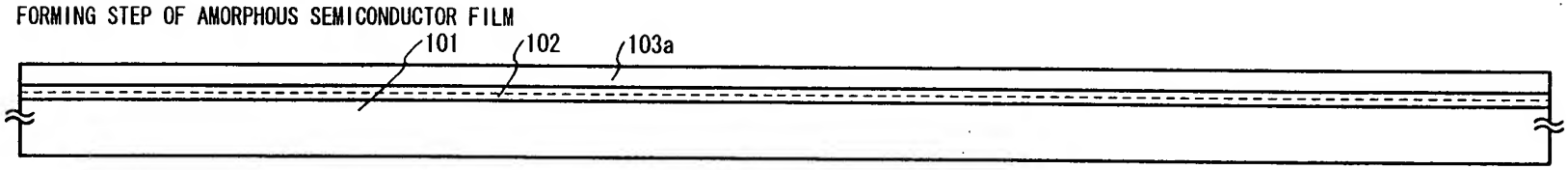


FIG. 1(B)

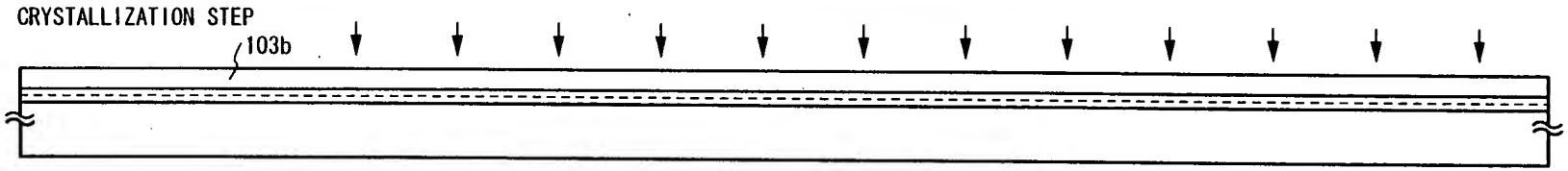


FIG. 1(C)

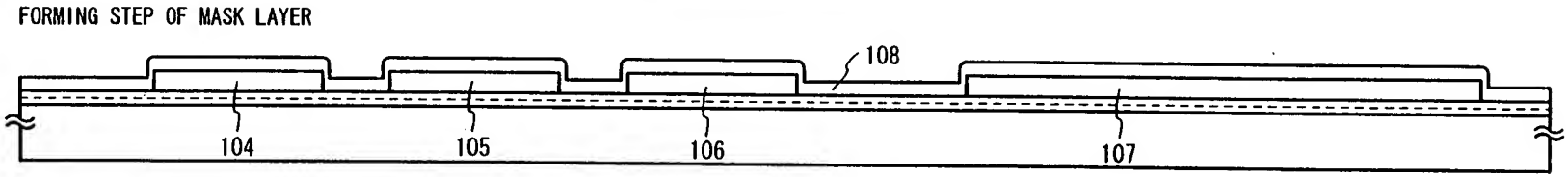


FIG. 1(D)

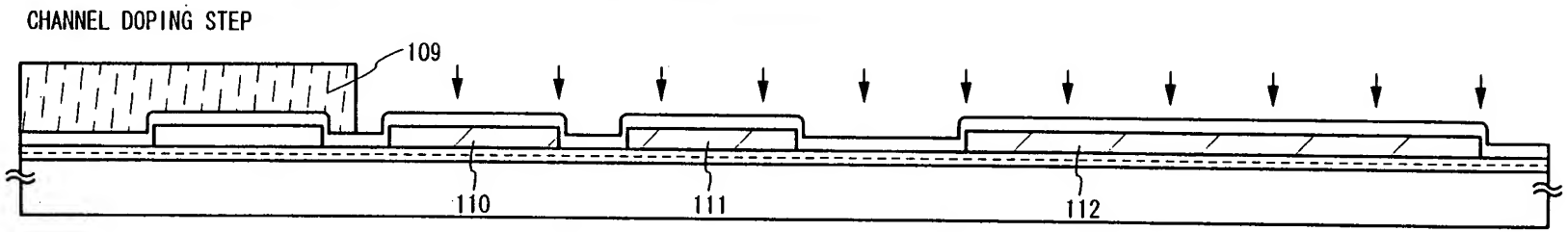


FIG. 2(A)

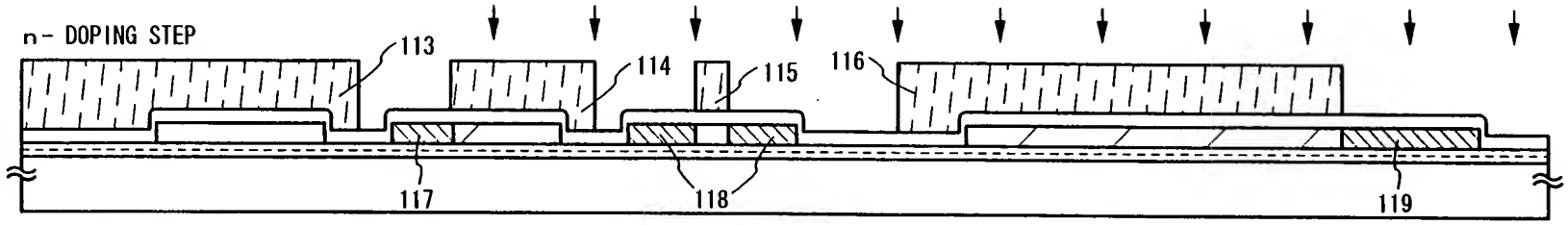


FIG. 2(B)

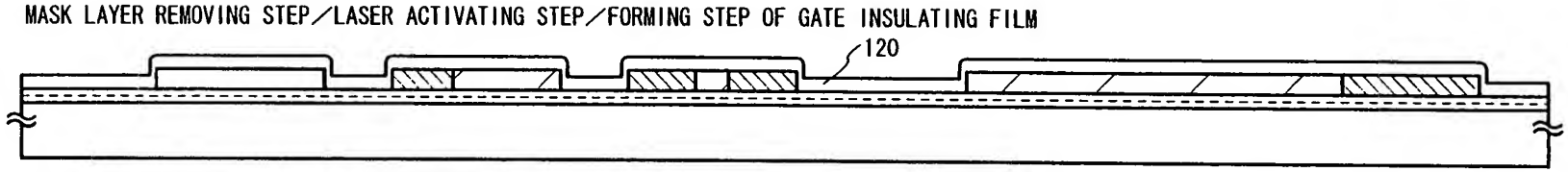


FIG. 2(C)

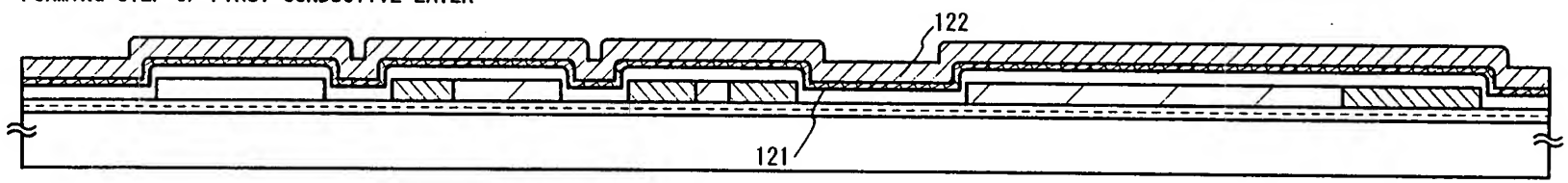


FIG. 2(D)

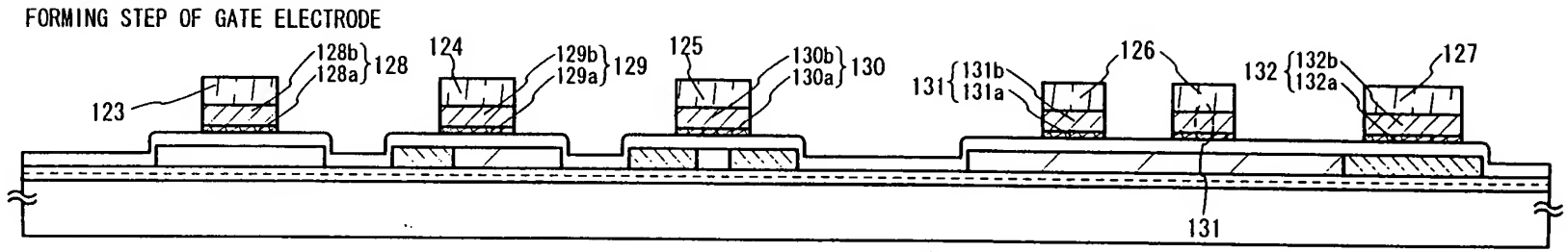


FIG. 3(A)

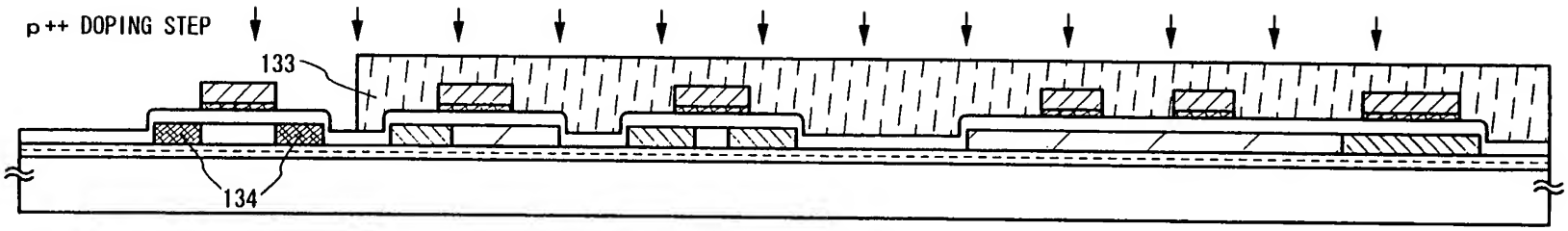


FIG. 3(B)

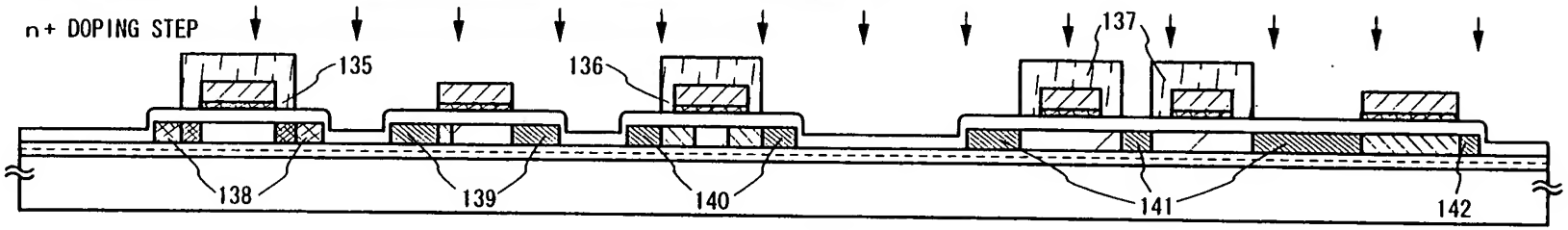


FIG. 3(C)

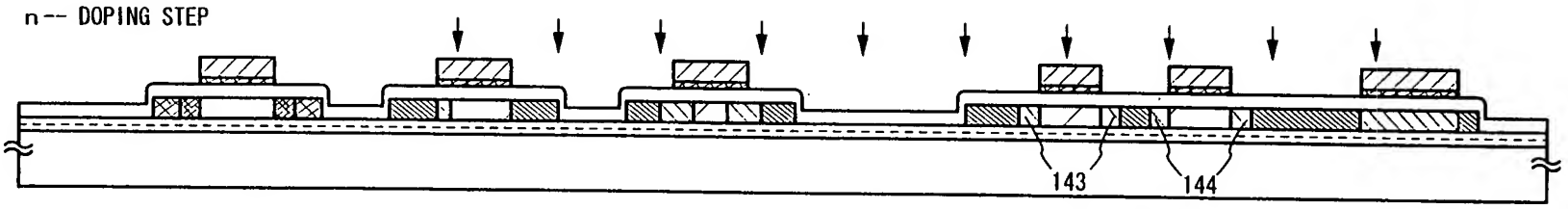


FIG. 3(D)

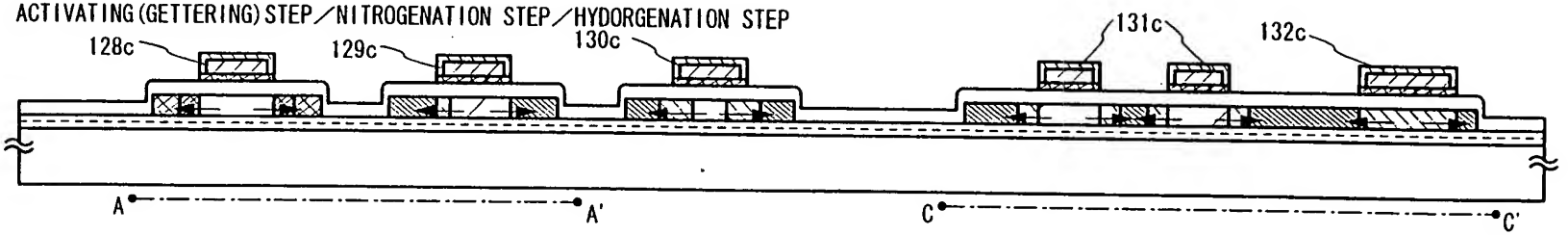


FIG. 4(A)

FORMING STEP OF SECOND CONDUCTIVE LAYER

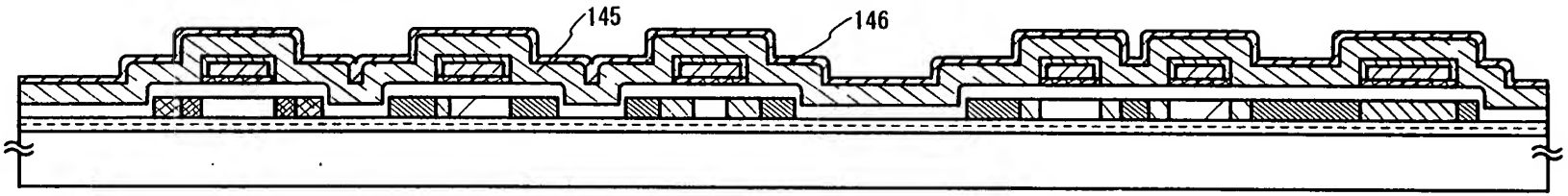


FIG. 4(B)

FORMING STEP OF GATE WIRING

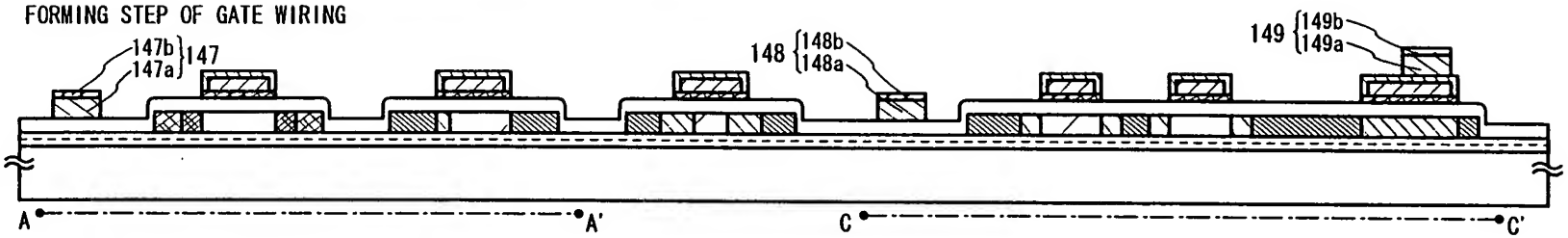
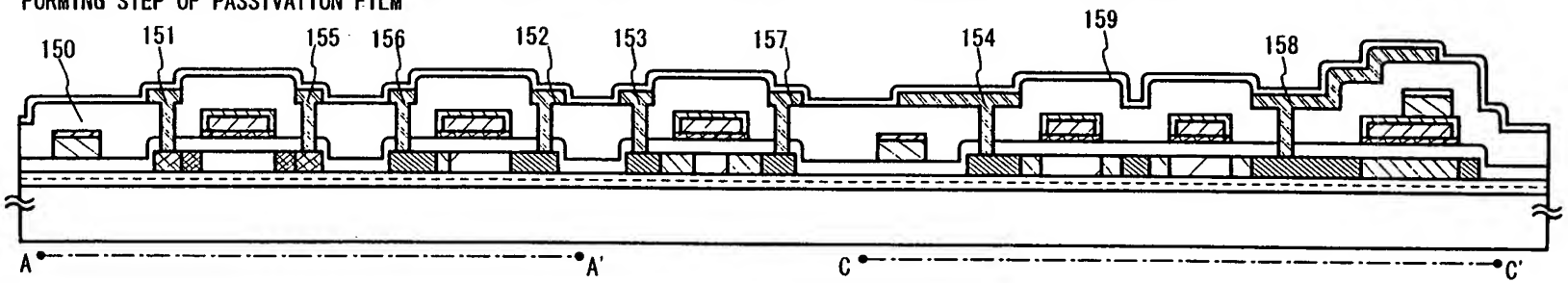


FIG. 4(C)

FORMING STEP OF INTERLAYER INSUALTING FILM/FORMING STEP OF CONTACT HOLE/FORMING STEP OF WIRING/
FORMING STEP OF PASSIVATION FILM



FORMING STEP OF RESIN FILM/FORMING STEP OF CONTACT HOLE/FORMING STEP OF PIXEL ELECTRODE

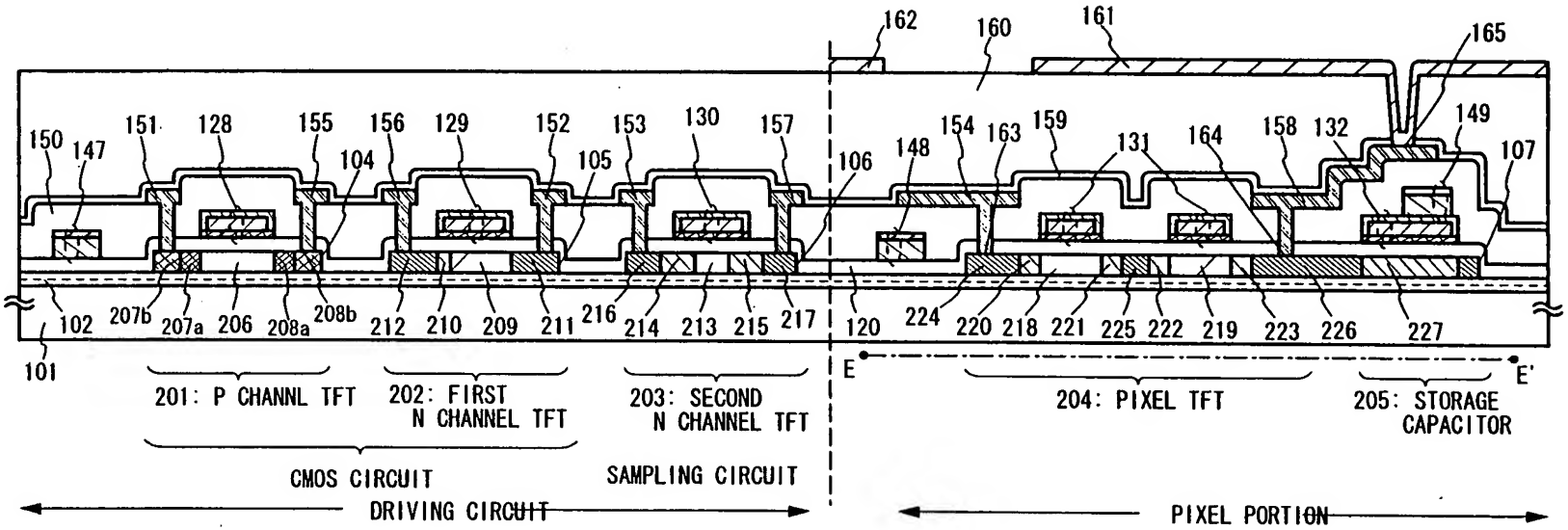


FIG. 5

FIG. 6(A)

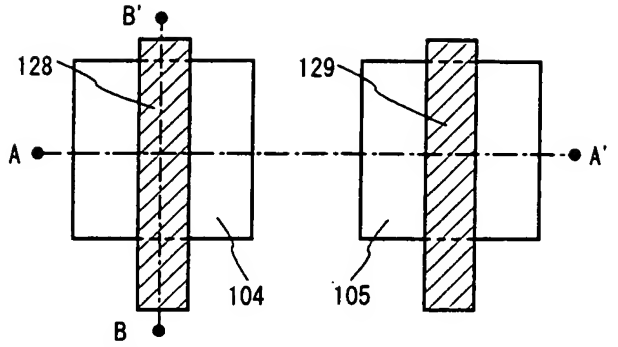


FIG. 6(B)

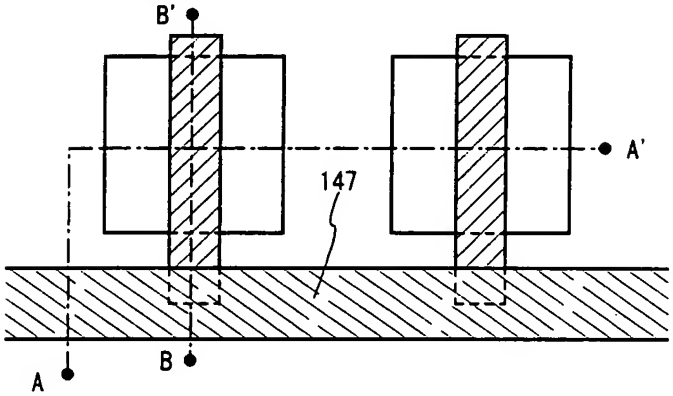


FIG. 6(C)

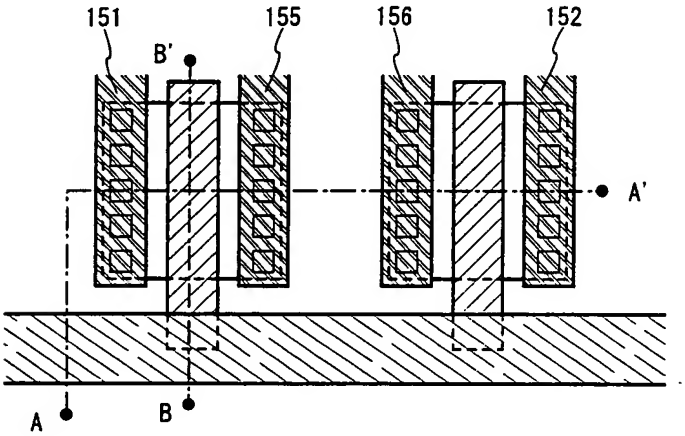


FIG. 7(A)

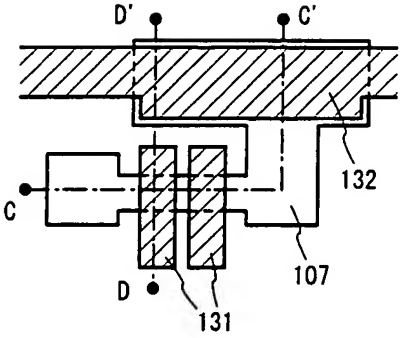


FIG. 7(B)

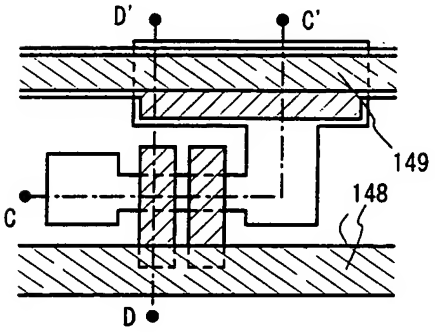


FIG. 7(C)

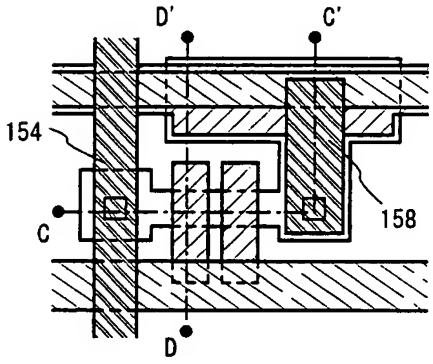


FIG. 8(A)

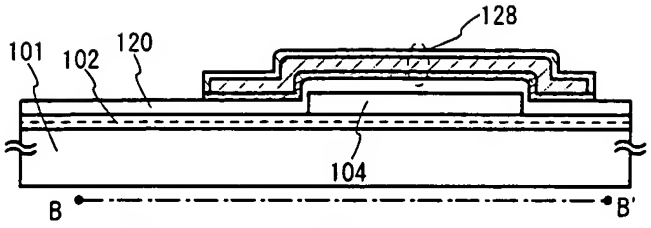


FIG. 8(B)

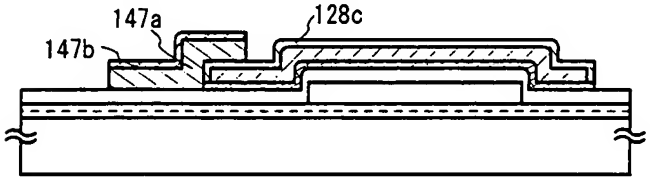


FIG. 8(C)

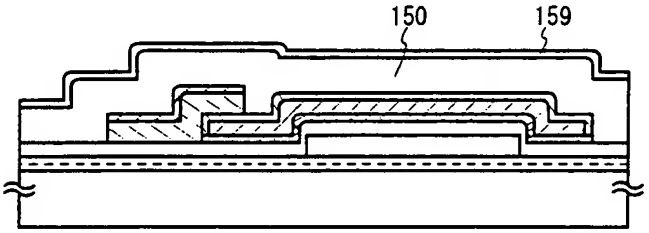


FIG. 9(A)

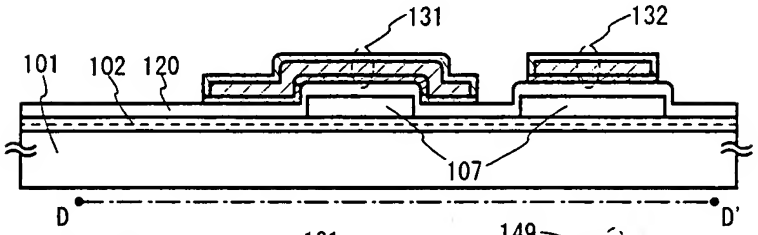


FIG. 9(B)

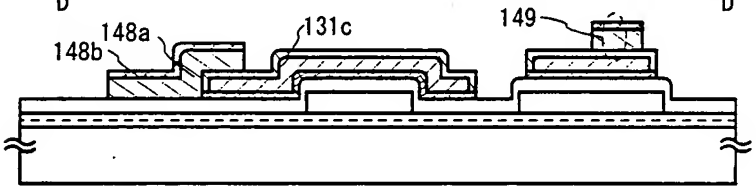
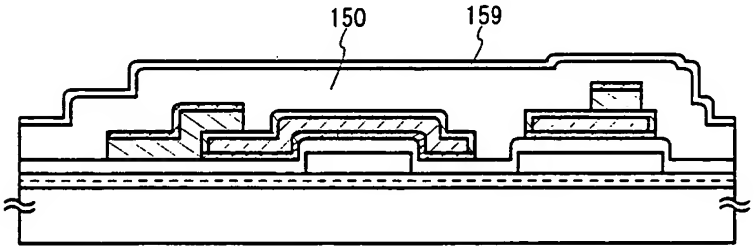


FIG. 9(C)



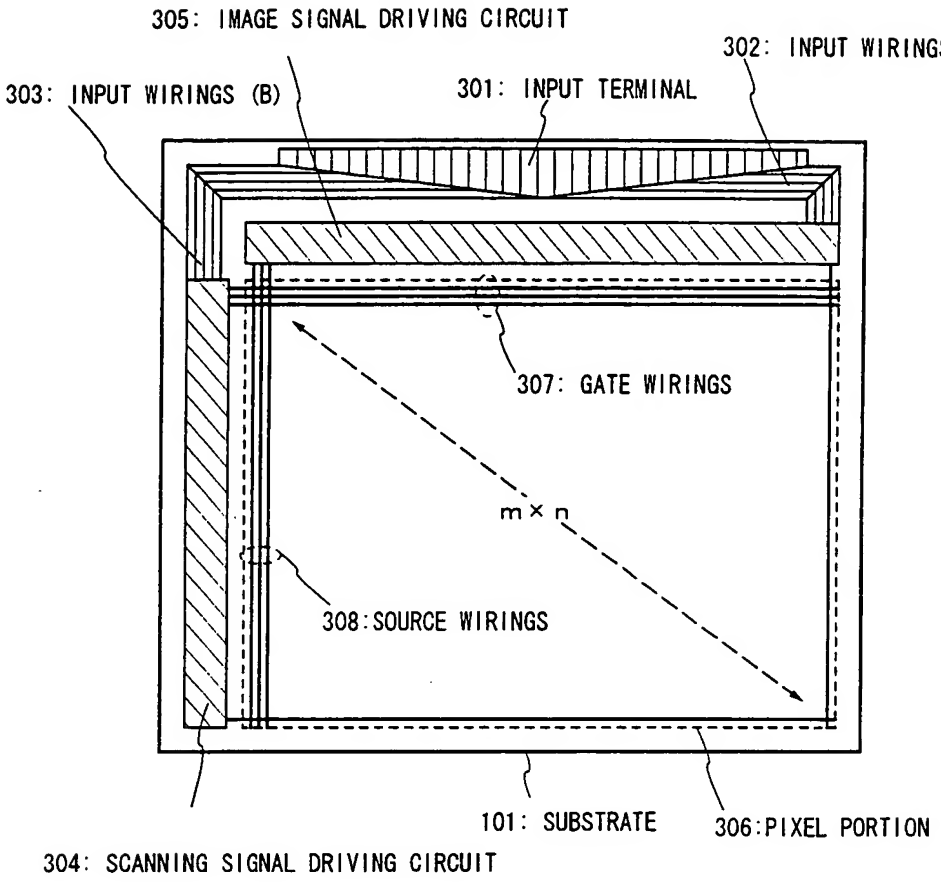

305: IMAGE SIGNAL DRIVING CIRCUIT
302: INPUT WIRINGS (A)
303: INPUT WIRINGS (B)
301: INPUT TERMINAL
307: GATE WIRINGS
m × n
308: SOURCE WIRINGS
101: SUBSTRATE
306: PIXEL PORTION
304: SCANNING SIGNAL DRIVING CIRCUIT

FIG. 10

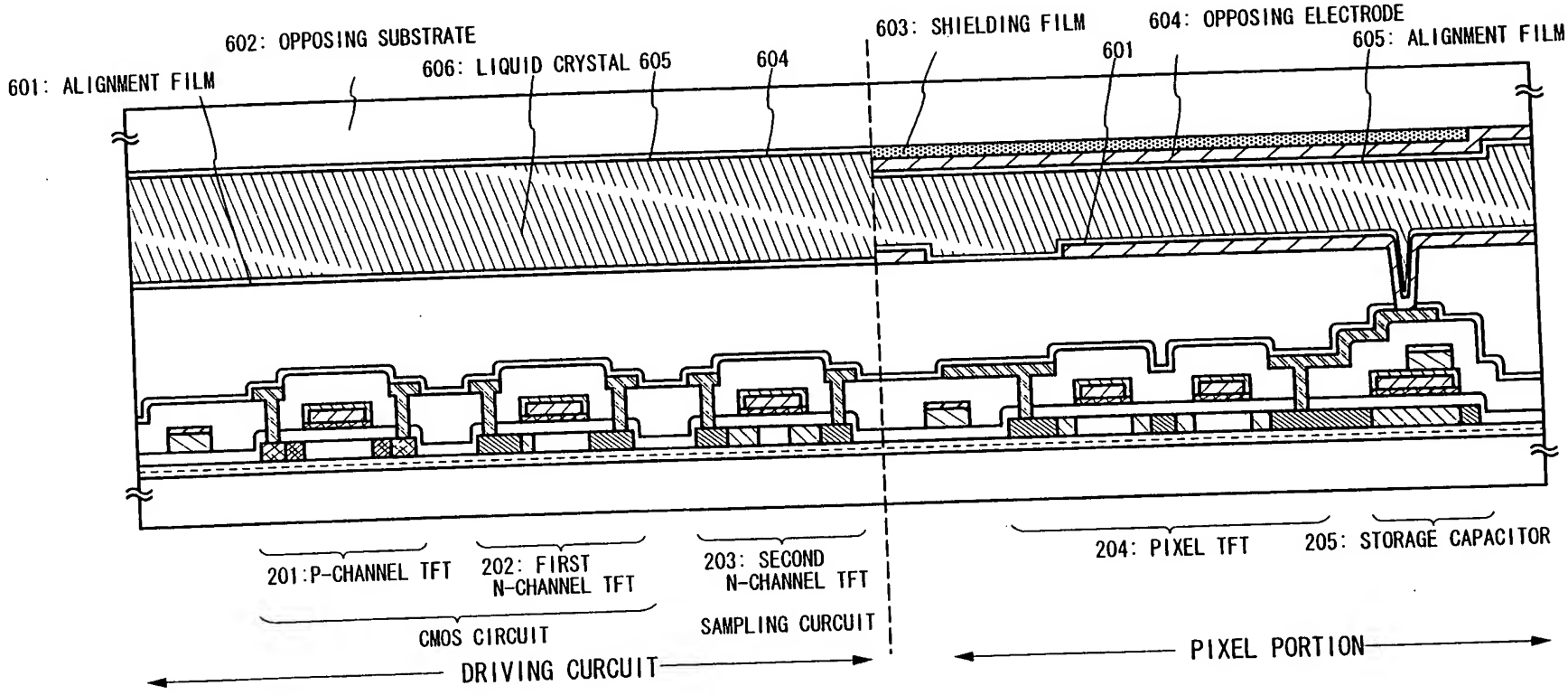

602: OPPOSING SUBSTRATE
601: ALIGNMENT FILM
606: LIQUID CRYSTAL 605
604
603: SHIELDING FILM
601
604: OPPOSING ELECTRODE
605: ALIGNMENT FILM
201:P-CHANNEL TFT
202: FIRST N-CHANNEL TFT
203: SECOND N-CHANNEL TFT
204: PIXEL TFT
205: STORAGE CAPACITOR
CMOS CIRCUIT
SAMPLING CURCUIT
DRIVING CURCUIT
PIXEL PORTION

FIG. 11

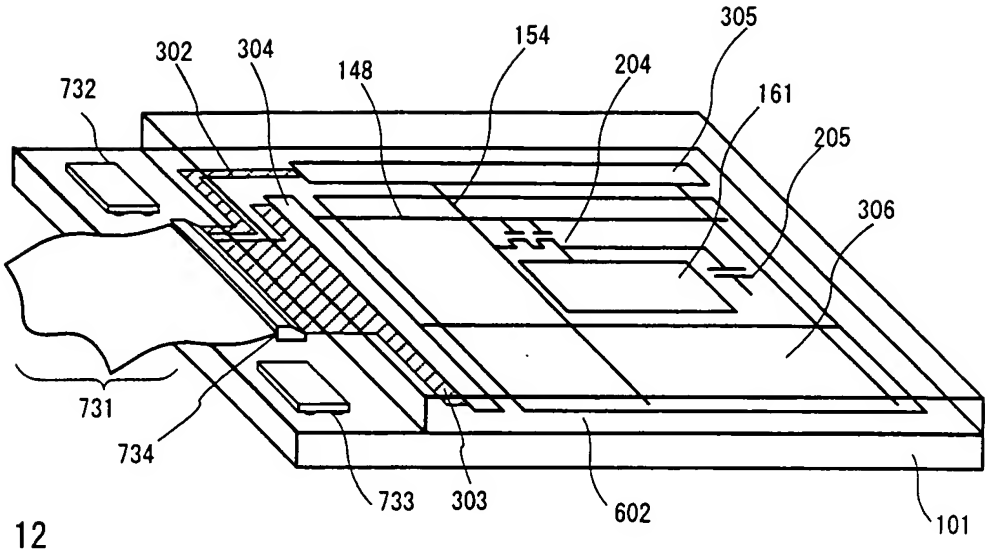


FIG. 12

101 : SUBSTRATE
306 : PIXEL PORTION
302, 303: INPUT WIRINGS
304 : SCANNING SIGNAL DRIVING CIRCUIT
305 : IMAGE SIGNAL DRIVING CIRCUIT
731 : FPC
732, 733 : IC CHIP
734 : external I/O terminal

204 : PIXEL TFT
148 : GATE WIRINGS
154 : SOURCE WIRINGS
161 : PIXEL ELECTRODE
205 : STORAGE CAPACITOR

602 : OPPOSING SUBSTRATE

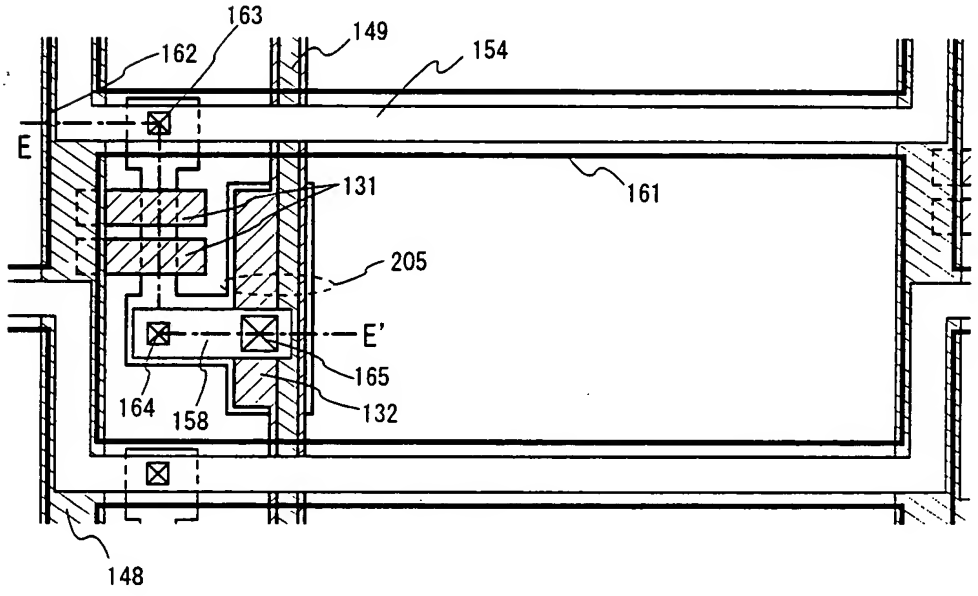


FIG. 13

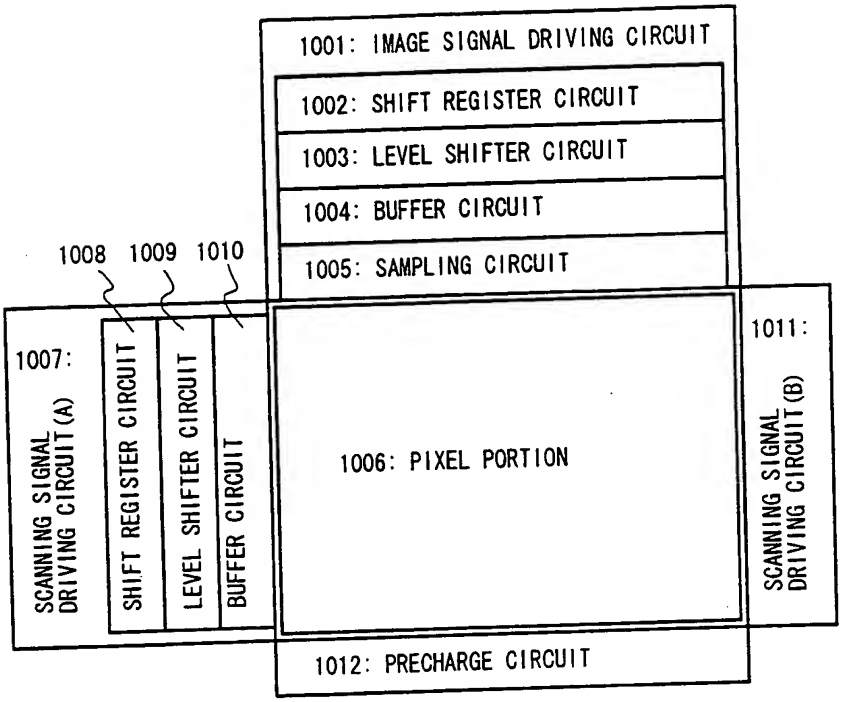


FIG. 14

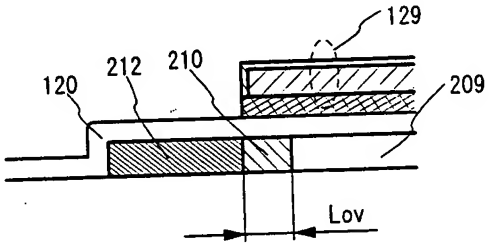


FIG. 15(A)

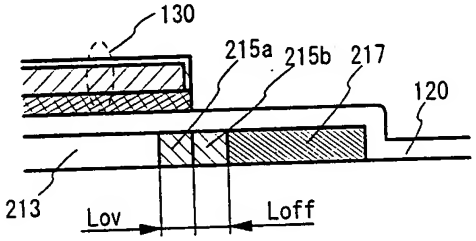


FIG. 15(B)

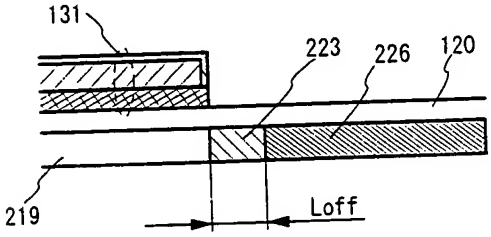


FIG. 15(C)

FIG. 16(A)

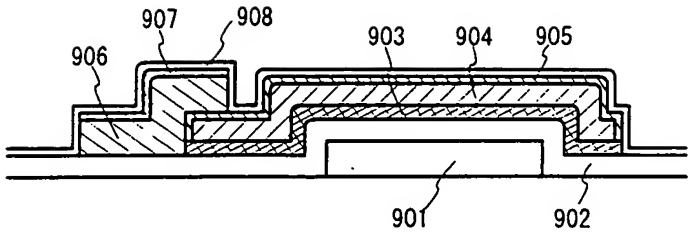


FIG. 16(B)

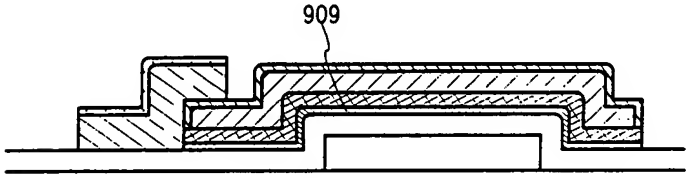
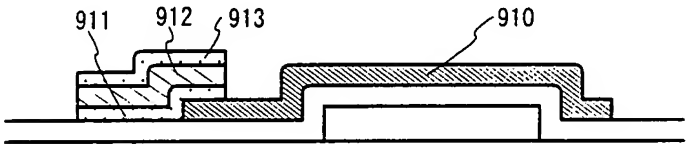


FIG. 16(C)



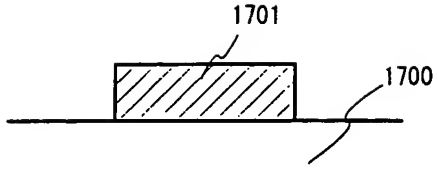


FIG. 17(A)

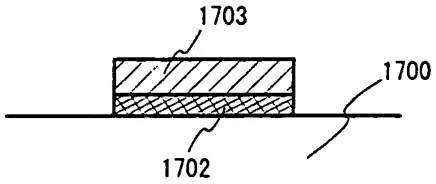


FIG. 17(B)

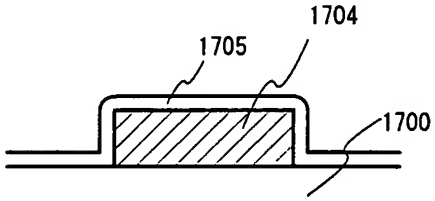


FIG. 17(C)

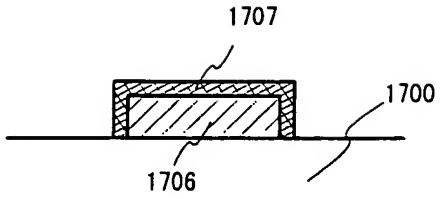


FIG. 17(D)

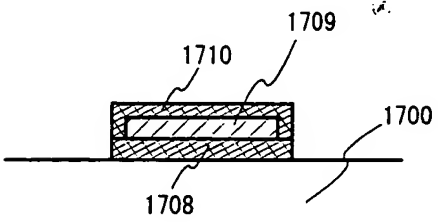


FIG. 17(E)

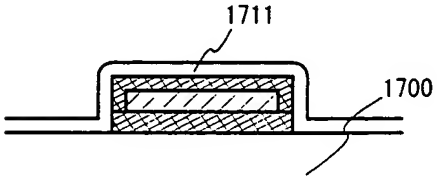


FIG. 17(F)

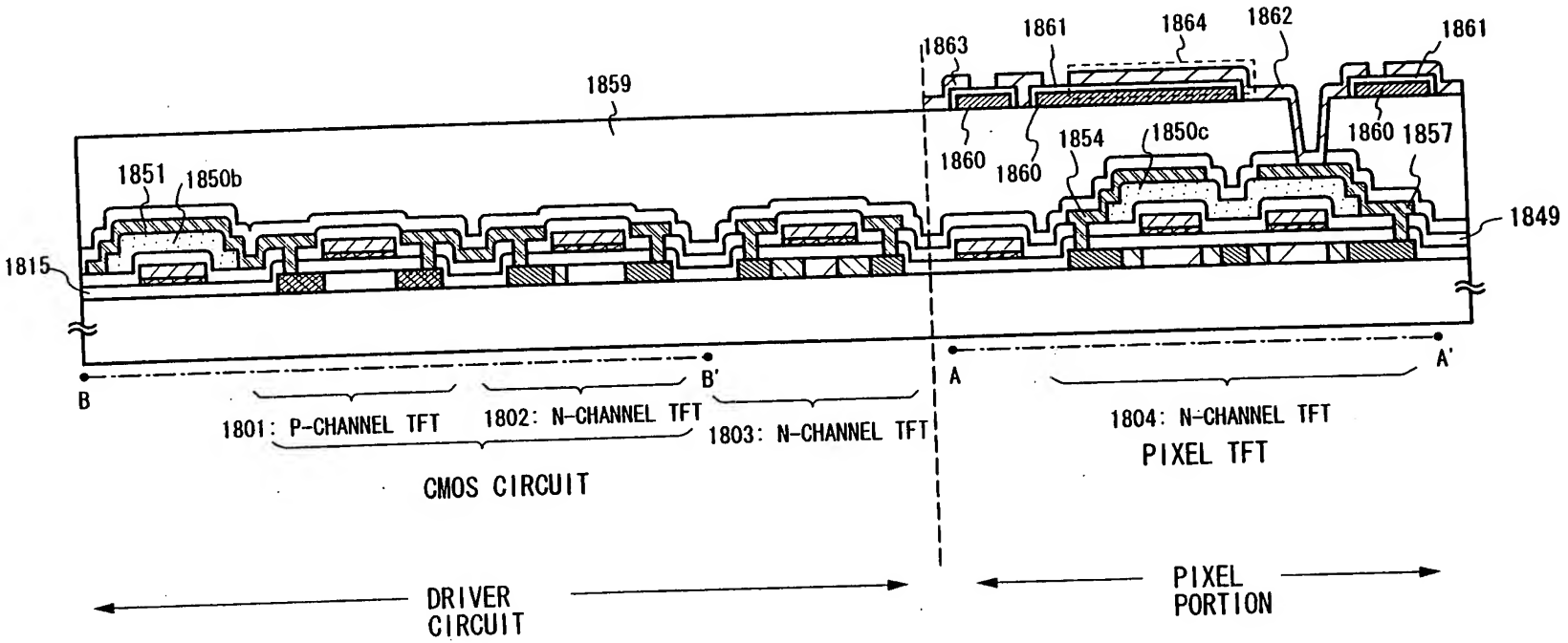

1861
1864
1862
1861
1863
1859
1860
1860
1854
1850c
1860
1857
1851
1850b
1849
1815
B
B'
A
A'
1801: P-CHANNEL TFT
1802: N-CHANNEL TFT
1803: N-CHANNEL TFT
1804: N-CHANNEL TFT
CMOS CIRCUIT
PIXEL TFT
DRIVER CIRCUIT
PIXEL PORTION

FIG. 18

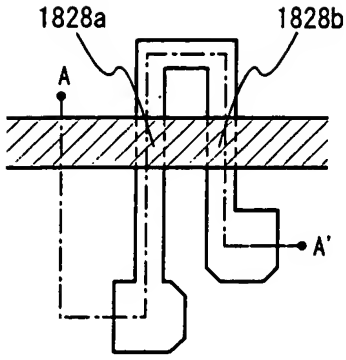


FIG. 19(A)

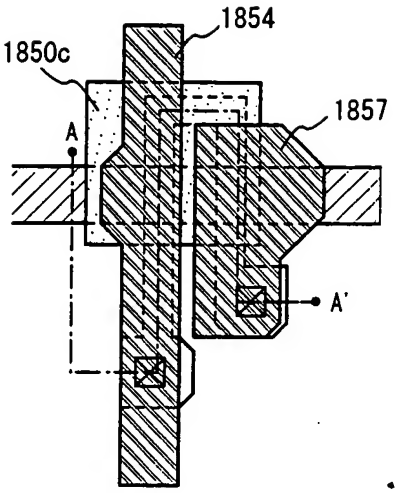


FIG. 19(B)

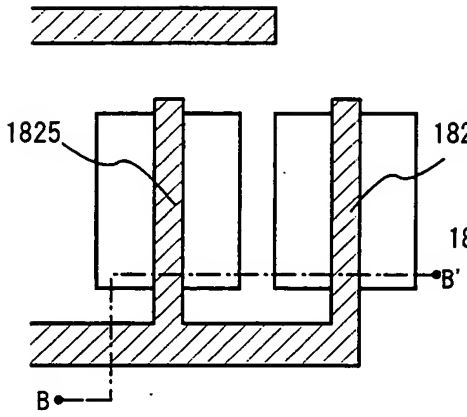


FIG. 20(A)

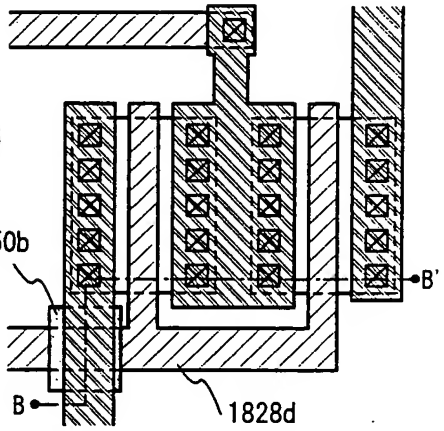


FIG. 20(B)

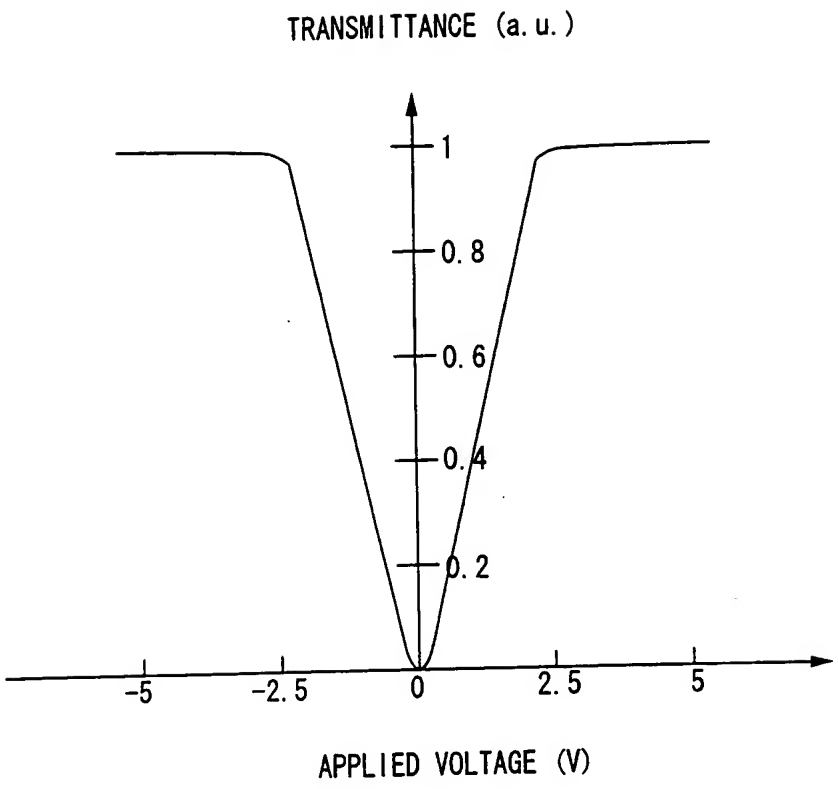
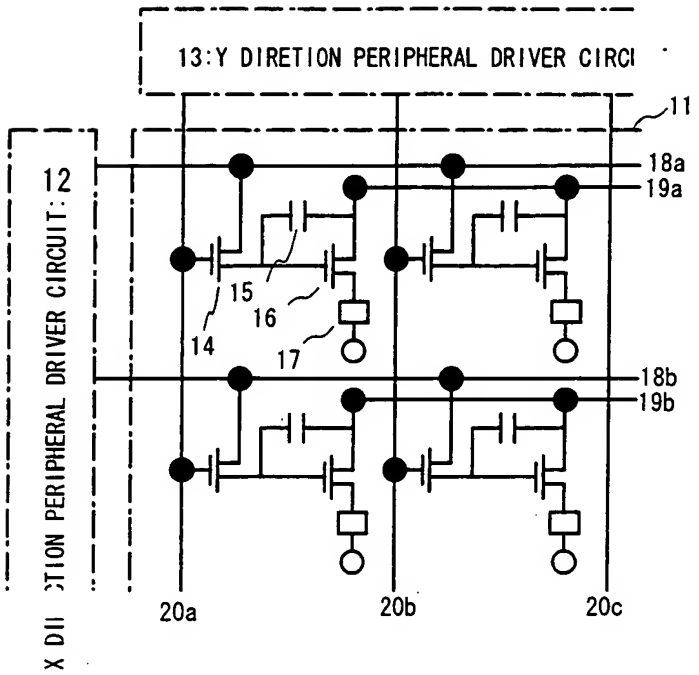


FIG. 21



11: PIXEL PORTION
12: X DIRECTION PERIPHERAL DRIVER CIRCUIT
13: Y DIRETION PERIPHERAL DRIVER CIRCUIT
14: SWITCHING TFT
15: STORAGE CAPACITOR
16: CURRENT CONTROLLING TFT
17: ORGANIC EL ELEMENT
18A, 18B: X-DIRECTION SIGNAL LINES
19A, 19B: POWER SUPPLY LINES
20A, 20B, 20C: Y-DIRECTION SIGNAL LINES

FIG. 22

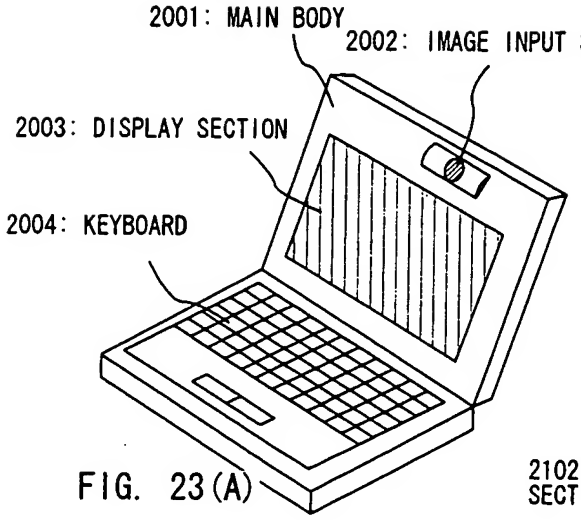


FIG. 23(A)

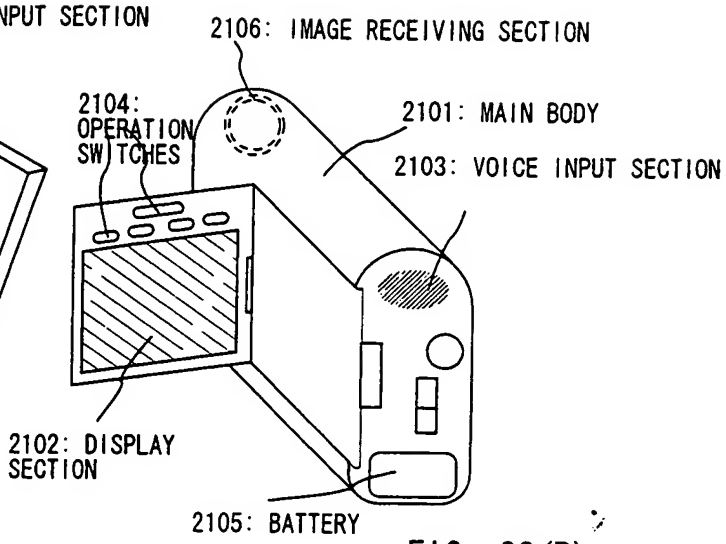


FIG. 23(B)

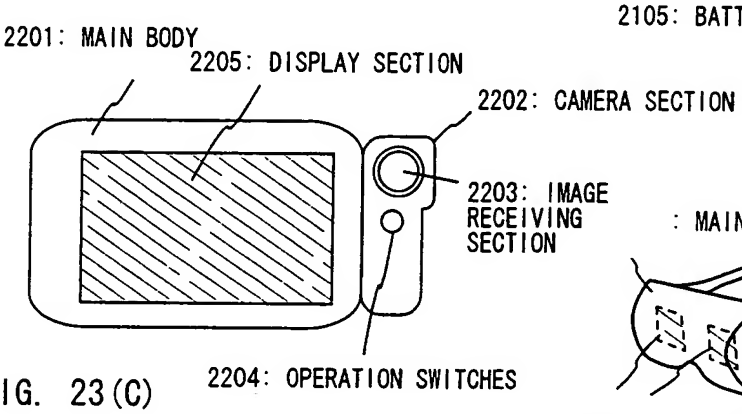


FIG. 23(C)

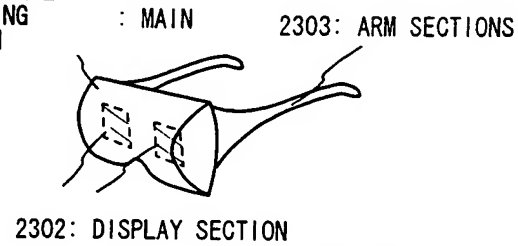


FIG. 23(D)

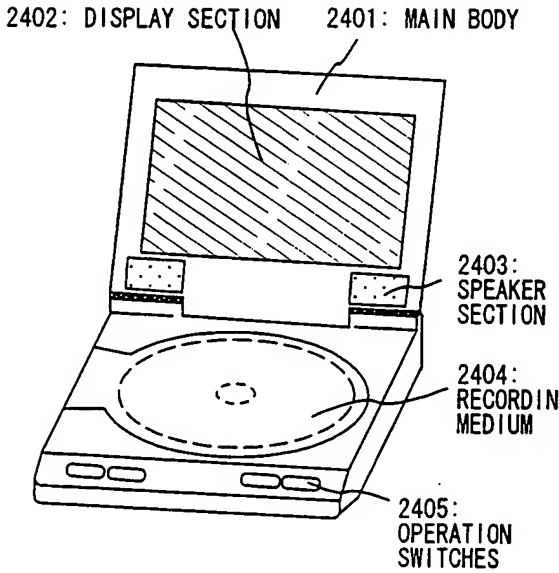


FIG. 23(E)

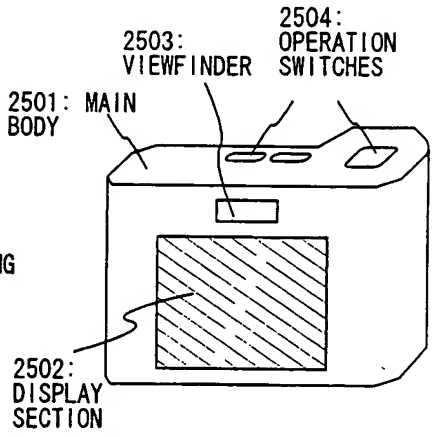


FIG. 23(F)

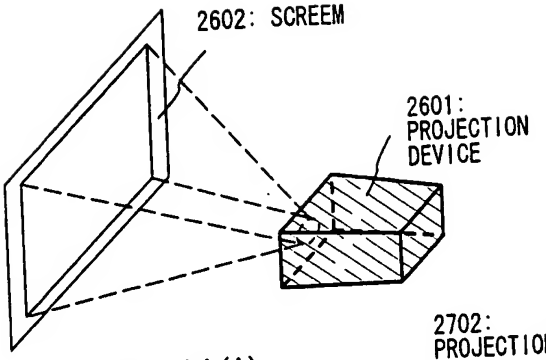


FIG. 24(A)

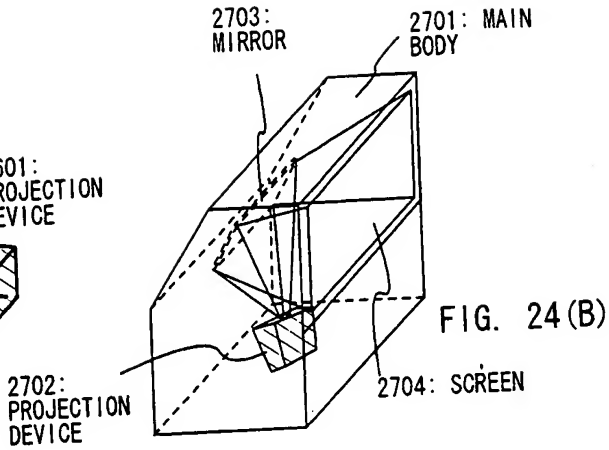


FIG. 24(B)

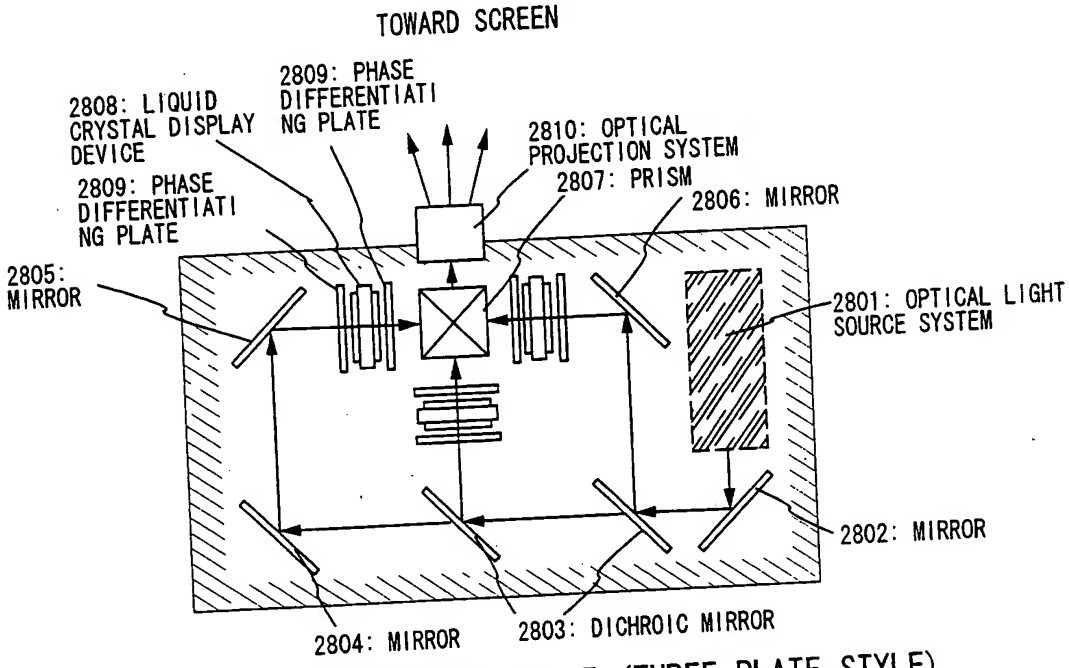


FIG. 24(C) PROJECTION DEVICE (THREE-PLATE STYLE)

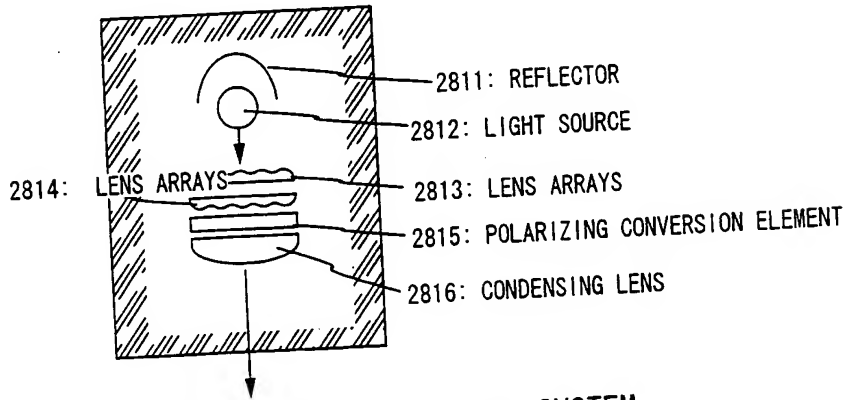


FIG. 24(D) OPTICAL LIGHT SOURCE SYSTEM

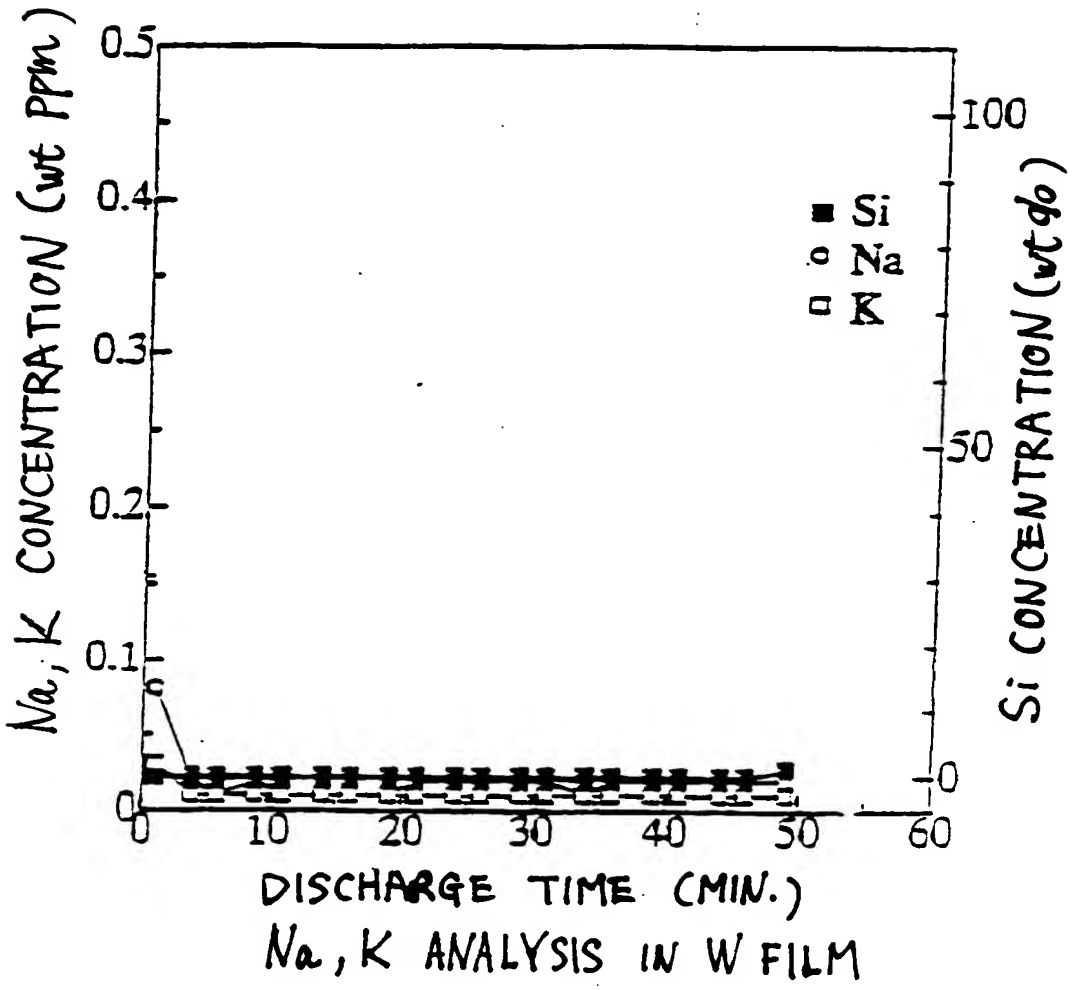

Na, K CONCENTRATION (wt PPM)
0.5
0.4
0.3
0.2
0.1
0
100
50
0
Si CONCENTRATION (wt %)
■ Si
○ Na
□ K
0
10
20
30
40
50
60
DISCHARGE TIME (MIN.)
Na, K ANALYSIS IN W FILM

FIG. 25

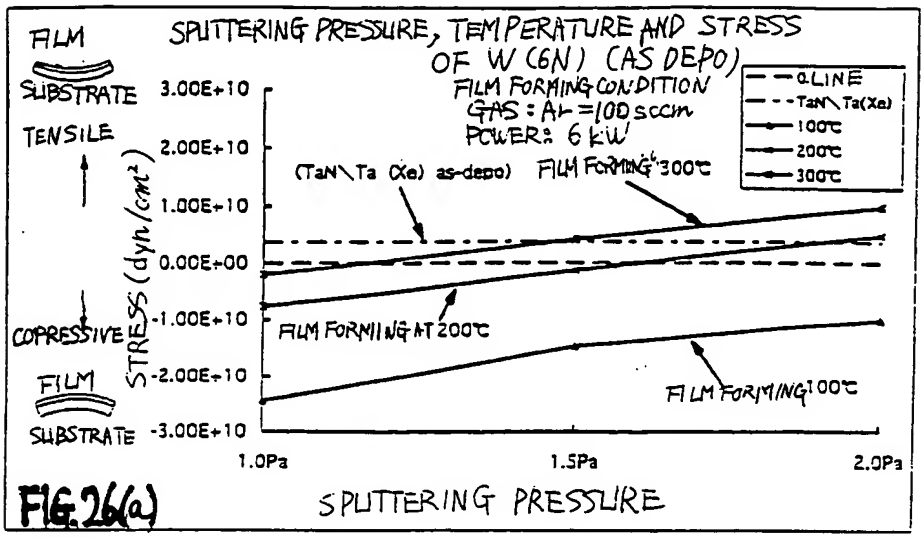


FIG. 26(a)

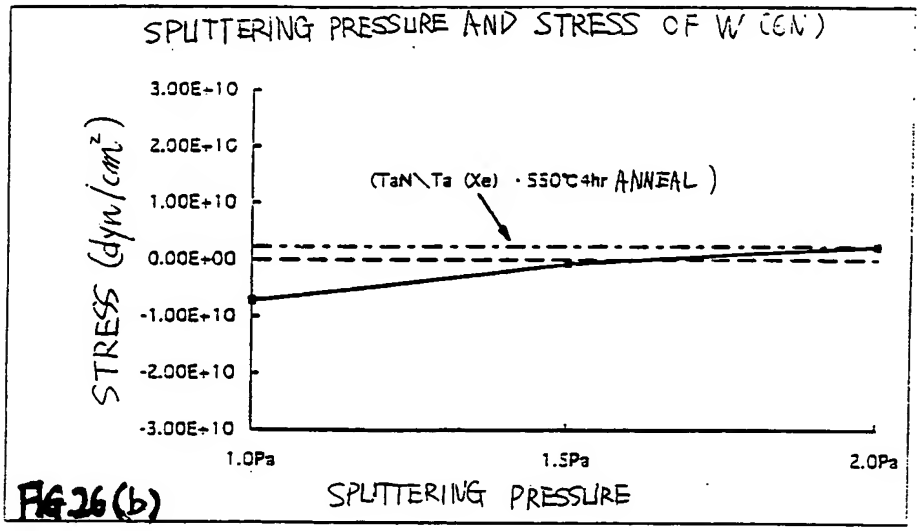


FIG. 26(b)

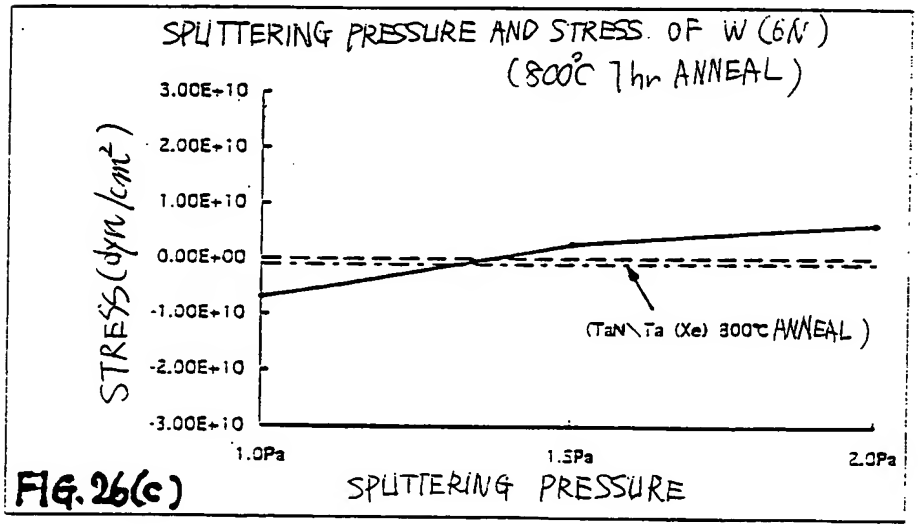


FIG. 26(c)

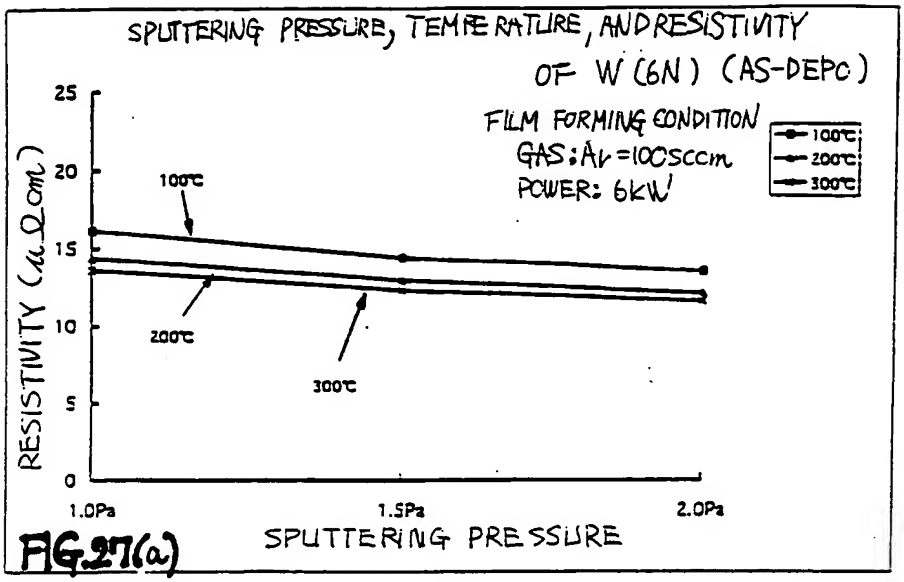


FIG.27(a)

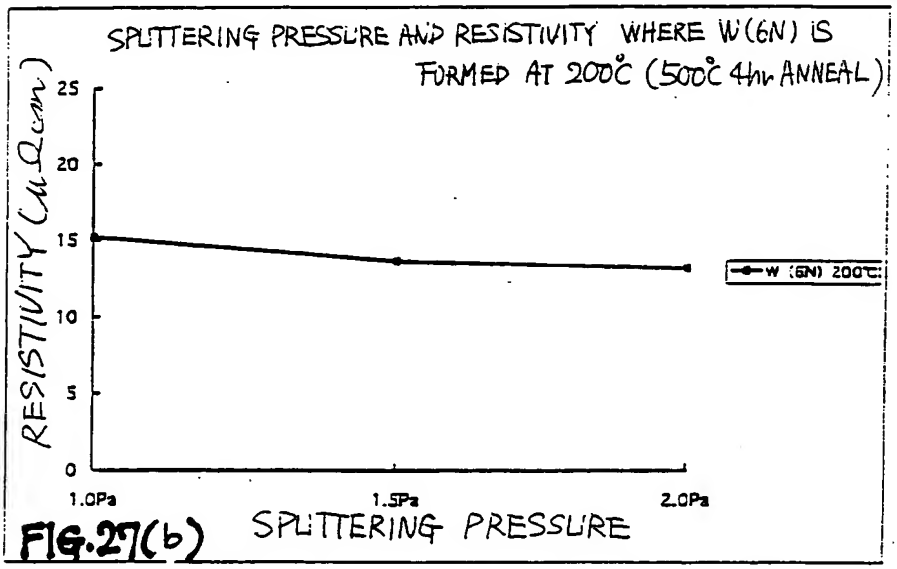


FIG.27(b)

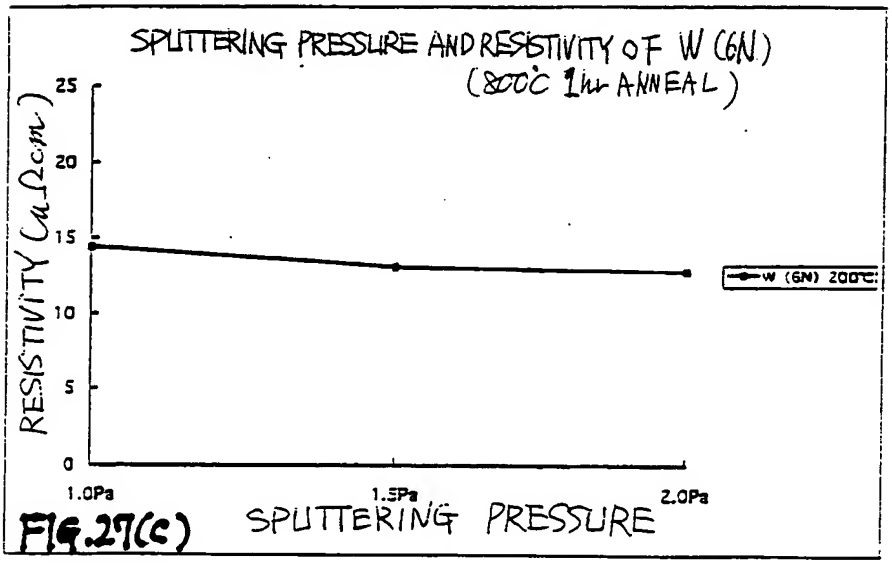


FIG.27(c)

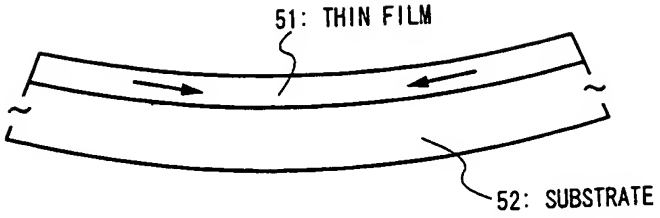


FIG. 28(A) TENSILE STRESS

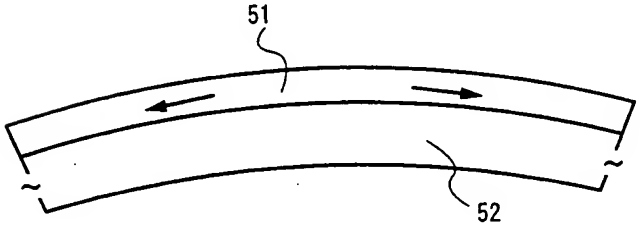


FIG. 28(B) COMPRESSIVE STRESS

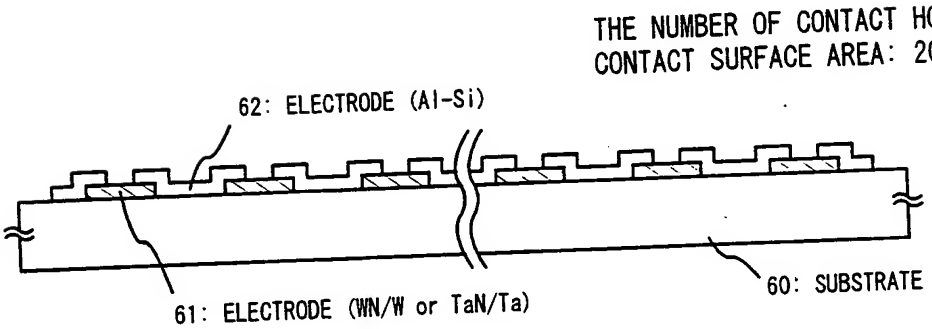
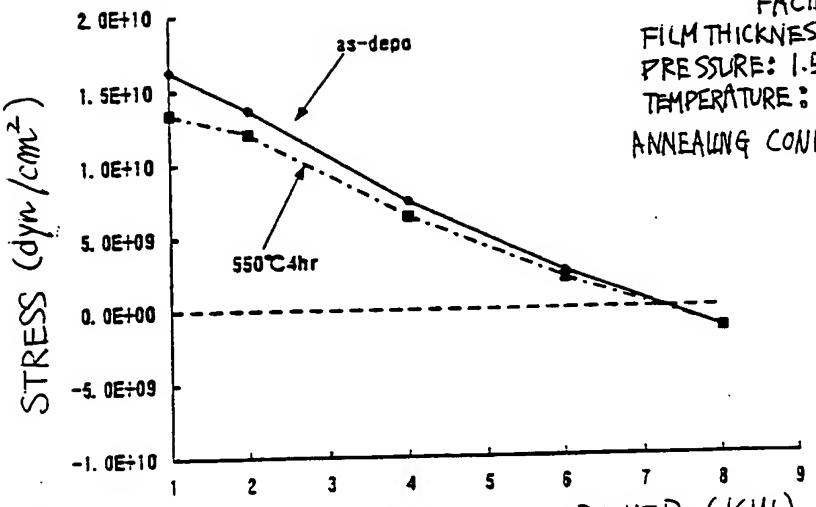


FIG. 29

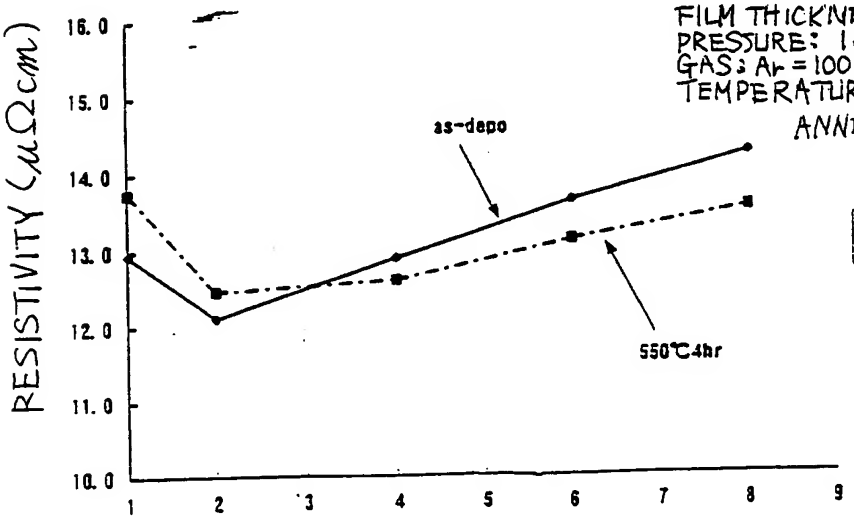


SPUTTERING CONDITION
DEVICE: SINGLE SUBSTRATE STYLE FACING SPUTTERING SYSTEM
FILM THICKNESS: 400nm
PRESSURE: 1.5 Pa
TEMPERATURE: 200℃
ANNEALING CONDITION (WITHOUT CAPPING)

as-depo
550℃4hr
0 LINE

FIG.30

W FILM FORMING POWER AND STRESS



SPUTTERING CONDITION
DEVICE: SINGLE SUBSTRATE STYLE FACING SPUTTERING SYSTEM
FILM THICKNESS: 400 nm
PRESSURE: 1.5 Pa
GAS: Ar = 100 sccm
TEMPERATURE: 200℃
ANNEALING CONDITION (WITHOUT CAPPING)

as-depo
550℃4hr

FIG.31

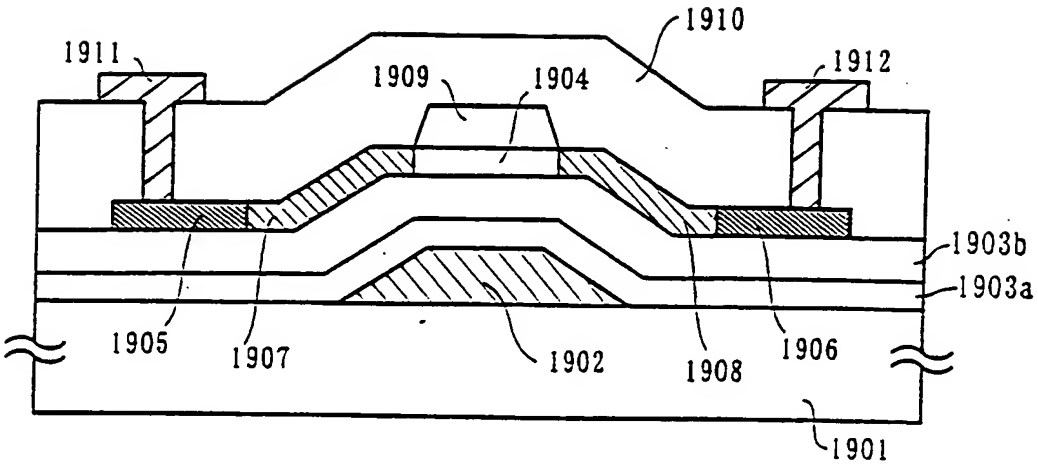

1910
1911
1912
1909
1904
1903b
1903a
1905
1907
1902
1908
1906
1901

FIG. 32